WHAT IS CLAIMED IS:

1. An apparatus for controlling a delay time of a signal in a semiconductor device, the apparatus comprising:

a test mode delay section for receiving a pulse signal and outputting first to (N+1)th control signals; and

a test delay section for delaying an input signal for a predetermined time by the first to the (N+1)th control signals and outputting the delayed signal,

wherein a delay time required for outputting the input signal as an output signal is controlled according to an enabled control signal from among the first to the (N+1)th control signals, the first to the (N+1)th control signals are sequentially enabled by the pulse signal, and, after the (N-1)th control signal is enabled, the Nth and the (N+1)th control signals are alternately enabled every time the pulse signal is toggled.

2. The apparatus for controlling a delay time of a signal in a semiconductor device as claimed in claim 1, wherein enabling points of the Nth and (N+1)th control signals are adjusted by adjusting an enabling point of the pulse signal.

3. The apparatus for controlling a delay time of a signal in a semiconductor device as claimed in claim 1, wherein, in a standby state, the first control signal is in an enabled state, and the second to the (N+1)th control signals are in a disabled state.

4. The apparatus for controlling a delay time of a signal in a semiconductor device as claimed in claim 1, wherein the test mode delay section further receives a reset signal, the first control signal is enabled and the second to the (N+1)th control signals are disabled when the reset signal is enabled.

5. The apparatus for controlling a delay time of a signal in a semiconductor device as claimed in claim 1, wherein the test delay section includes first to Nth delay devices sequentially connected to each other and first to Nth switch devices, the Nth switch device is connected between an output terminal of the first delay device and a first node, the first to the (N-1)th delay devices are respectively connected between each output terminal of the second to the Nth delay devices and first node, the input signal is received at an input terminal of the first delay device, and each of the first to the Nth switch devices is turned on/off

in response to the first to the Nth control signals.

6. The apparatus for controlling a delay time of a signal in a semiconductor device as claimed in claim 5, wherein the (N+1)th control signal is received by the (N+1)th switch device connected between the input terminal of the first delay device and the first node, and the (N+1)th switch device is always in a turned-off state.

7. The apparatus for controlling a delay time of a signal in a semiconductor device as claimed in claim 1, wherein the test mode delay section includes first to Nth shift units, the first control signal is outputted from an input terminal of the first shift unit, the second to the (N+1)th control signals are respectively outputted from each output terminal of the first to the Nth shift units, and the (N+1)th control signal is applied to an input terminal of the (N-1)th shift unit through a latch means, in order to allow the Nth control signal and the (N+1)th control signal to be alternately enabled, every time the pulse signal is toggled after the (N-1)th control signal is enabled.

8. The apparatus for controlling a delay time of a signal in a semiconductor device as claimed in claim 7,

wherein, in a standby state, the first control signal is in an enabled state, and the second to the (N+1)th control signal are in a disabled state.

9. The apparatus for controlling a delay time of a signal in a semiconductor device as claimed in claim 8, wherein a logic level stored in an each shift unit is sequentially transmitted to next shift unit every time the pulse signal is toggled.

10. A method for controlling a delay time of a signal in a semiconductor device, the method comprising the steps of:

a) applying a test mode pulse signal;

b) generating N number of test mode selection signals which are synchronized with the falling edges of the test mode pulse signal to respond sequentially;

c) sequentially regenerating the (N-1)th test mode selection signal after the Nth test mode selection signal is generated; and

d) repeating step c, wherein an input signal inputted to the semiconductor device is delayed by a predetermined time to be outputted as an output signal only when first to the (N-1)th test mode selection signals are enabled, and the delayed times are different from each other according to the

first to the (N-1)th test mode selection signals.

11. A method for controlling a delay time of a signal in a semiconductor device as claimed in claim 10, wherein a falling point of the test mode pulse signal is adjusted, so as to adjust pulse widths of the Nth and the (N-1)th test mode selection signals, thereby adjusting the delayed time required for outputting the input signal as the output signal.

12. A method for controlling a delay time of a signal in a semiconductor device as claimed in claim 10, wherein step b includes the substeps of:

b-1) shifting the first test mode selection signal, which maintains a standby state of a high level, to a lower level and a second test mode selection signal to a high level when a first falling edge of the test mode pulse signal occurs,

b-2) shifting the second test mode selection signal at a high level to a lower level and a third test mode selection signal to a high level when a second falling edge of the test mode pulse signal occurs,

b-3) shifting the third test mode selection signal at a high level to a lower level and a fourth test mode

selection signal to a high level when a third falling edge of the test mode pulse signal occurs,

b-4) b-2) and b-3) are employed in the fifth to the Nth test mode selection signal.

13. A method for controlling a delay time of a signal in a semiconductor device as claimed in claim 12, wherein each of high level pulse widths of the second to the (N-1)th test mode selection signals is the same as a period of the test mode pulse signal generating the second to the (N-1)th test mode selection signals.